UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/810,431	03/26/2004	Stephen Strickland	EMC04-02(04012)	9773

47653 7590 07/26/2006

DAVID E. HUANG, ESQ.
BAINWOOD HUANG AND ASSOCIATES LLC
2 CONNECTOR ROAD
WESTBOROUGH, MA 01581

EXAMINER	
SUGENT, JAMES F	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 07/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/810,431	STRICKLAND, STEPHEN	
	Examiner	Art Unit	
	James F. Sugent	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *May 31, 2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is sent in response to Applicant's Communication received March 26, 2004 for application number 10/810431. The Office hereby acknowledges receipt of the following and placed of record in file: Information Disclosure Statement (IDS) and claims 1-20 which are presented for examination.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on March 31, 2005 was filed. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 6, 13 and 14 rejected under 35 U.S.C. 103(a) as being unpatentable over Amin et al. (U.S. Patent No. 6,333,650 B1) (hereinafter referred to as Amin) in view of Brown et al. (U.S. Patent No. 6,879,139 B2) (hereinafter referred to as Brown).

As to claim 1, Amin discloses a data storage system (column 2, lines 49-51), comprising: power circuitry configured to provide power signals (130); storage processing circuitry

configured to perform data storage operations (101); and, a packaged microcontroller (103) coupled to the power circuitry and the storage processing circuitry (as shown in fig. 1), the packaged microcontroller having a set of input lines (Vin and input from 135), a set of output lines (from 120, 121 and 122), and control circuitry (123) coupled to the set of input lines and the set of output lines (as shown in fig. 1), the control circuitry being configured to: receive, on the set of input lines, a first set of power signals which is provided by the power circuitry to the storage processing circuitry (Amin discloses the power source 130 applying power Vin at start-up of the system and supplying a power input signal from 120 to electrical circuit 101; column 3, lines 35-44); wait a predetermined time period in response to receipt of the first set of power signals on the set of input lines (column 3, lines 45-47); and output a set of enable signals to the power regulators (120-122) after waiting the predetermined time period, the set of enable signals directing the power regulators to provide a second set of power signals to the storage processing circuitry (Amin discloses the control component 123 applying enable signal to the power regulator 121 after a pre-determined time period to electrical circuit 101; column 3, lines 53-57).

Amin fails to disclose the control circuit outputting, through the set of output lines, a set of enable signals to the power circuitry to delivery a second power signal to the storage processing circuit.

Brown teaches a power sequencing method and system comprising power circuitry (10). Brown continues to teach the power circuitry receiving enable signals from power control circuitry (collective switched mode power supplies 1-6) to enable the power to deliver the next power level signal via power control circuitry (1-6) (see figs. 1 and 2; column 4, lines 38-52 and

column 6, lines 1-11). Brown has the additional feature of disabling power supplies when faults are detected (column 3, lines 41-52).

It would have been obvious to one of ordinary skill of the art having the teachings of Amin and Brown at the time the invention was made, to modify power circuit of Amin to include receiving enable signals from a control circuitry and outputting power signals to processing circuitry as taught by Brown. One of ordinary skill in the art would be motivated to make this combination of having a power circuit receive enable signals from a control circuitry and outputting power signals to processing circuitry in view of the teachings of Brown, as doing so would give the added benefit of disabling power supplies when faults are detected (as taught by Brown above).

As to claim 6, Amin discloses a packaged microcontroller for controlling a data storage system (column 2, lines 49-51) having (i) power circuitry for providing power signals (130) and (ii) storage processing circuitry for performing data storage operations (101), the packaged microcontroller (103) comprising: a set of input lines (Vin and input from 135); a set of output lines (from 120, 121 and 122); and control circuitry (123) coupled to the set of input lines and the set of output lines (as shown in fig. 1), the control circuitry being configured to: receive, on the set of input lines, a first set of power signals which is provided by the power circuitry to the storage processing circuitry (Amin discloses the power source 130 applying power Vin at start-up of the system and supplying a power input signal from 120 to electrical circuit 101; column 3, lines 35-44); wait a predetermined time period in response to receipt of the first set of power signals on the set of input lines (column 3, lines 45-47); and output a set of enable signals to the power regulators (120-122) after waiting the predetermined time period, the set of enable signals

directing the power regulators to provide a second set of power signals to the storage processing circuitry (Amin discloses the control component 123 applying enable signal to the power regulator 121 after a pre-determined time period to electrical circuit 101; column 3, lines 53-57).

Amin fails to disclose the control circuit outputting, through the set of output lines, a set of enable signals to the power circuitry to delivery a second power signal to the storage processing circuit.

Brown teaches a power sequencing method and system comprising power circuitry (10). Brown continues to teach the power circuitry receiving enable signals from power control circuitry (collective switched mode power supplies 1-6) to enable the power to deliver the next power level signal via power control circuitry (1-6) (see figs. 1 and 2; column 4, lines 38-52 and column 6, lines 1-11). Brown has the additional feature of disabling power supplies when faults are detected (column 3, lines 41-52).

It would have been obvious to one of ordinary skill of the art having the teachings of Amin and Brown at the time the invention was made, to modify power circuit of Amin to include receiving enable signals from a control circuitry and outputting power signals to processing circuitry as taught by Brown. One of ordinary skill in the art would be motivated to make this combination of having a power circuit receive enable signals from a control circuitry and outputting power signals to processing circuitry in view of the teachings of Brown, as doing so would give the added benefit of disabling power supplies when faults are detected (as taught by Brown above).

As to claim 13, Amin discloses a packaged microcontroller for controlling a data storage system (column 2, lines 49-51) having (i) power circuitry for providing power signals (130) and

(ii) storage processing circuitry for performing data storage operations (101), the packaged microcontroller (103) comprising: a set of input lines (Vin and input from 135); a set of output lines (from 120, 121 and 122); and, control circuitry (123) coupled to the set of input lines and the set of output lines (as shown in fig. 1), the control circuitry including: means for receiving (123), on the set of input lines, a first set of power signals which is provided by the power circuitry to the storage processing circuitry (Amin discloses the power source 130 applying power Vin at start-up of the system and supplying a power input signal from 120 to electrical circuit 101; column 3, lines 35-44); means for waiting (129) a predetermined time period in response to receipt of the first set of power signals on the set of input lines (column 3, lines 45-47); and, means for outputting (123) a set of enable signals to the power regulators (120-122) after waiting the predetermined time period, the set of enable signals directing the power regulators to provide a second set of power signals to the storage processing circuitry (Amin discloses the control component 123 applying enable signal to the power regulator 121 after a pre-determined time period to electrical circuit 101; column 3, lines 53-57).

Amin fails to disclose a means for outputting, through the set of output lines, a set of enable signals to the power circuitry to delivery a second power signal to the storage processing circuit.

Brown teaches a power sequencing method and system comprising power circuitry (10). Brown continues to teach the power circuitry receiving enable signals from power control circuitry (collective switched mode power supplies 1-6) to enable the power to deliver the next power level signal via power control circuitry (1-6) (see figs. 1 and 2; column 4, lines 38-52 and

column 6, lines 1-11). Brown has the additional feature of disabling power supplies when faults are detected (column 3, lines 41-52).

It would have been obvious to one of ordinary skill of the art having the teachings of Amin and Brown at the time the invention was made, to modify power circuit of Amin to include receiving enable signals from a control circuitry and outputting power signals to processing circuitry as taught by Brown. One of ordinary skill in the art would be motivated to make this combination of having a power circuit receive enable signals from a control circuitry and outputting power signals to processing circuitry in view of the teachings of Brown, as doing so would give the added benefit of disabling power supplies when faults are detected (as taught by Brown above).

As to claim 14, Amin discloses in a packaged microcontroller (103), a method for controlling a data storage system (column 2, lines 49-51) having (i) power circuitry for providing power signals (130) and (ii) storage processing circuitry for performing data storage operations (101), the method comprising: receiving, on a set of input lines of the packaged microcontroller, a first set of power signals which is provided by the power circuitry to the storage processing circuitry (Amin discloses the power source 130 applying power Vin at start-up of the system and supplying a power input signal from 120 to electrical circuit 101; column 3, lines 35-44); waiting a predetermined time period in response to receipt of the first set of power signals on the set of input lines (column 3, lines 45-47); and outputting a set of enable signals to the power regulators (120-122) after waiting the predetermined time period, the set of enable signals directing the power regulators to provide a second set of power signals to the storage processing circuitry

(Amin discloses the control component 123 applying enable signal to the power regulator 121 after a pre-determined time period to electrical circuit 101; column 3, lines 53-57).

Amin fails to disclose the control circuit outputting, through the set of output lines, a set of enable signals to the power circuitry to delivery a second power signal to the storage processing circuit.

Brown teaches a power sequencing method and system comprising power circuitry (10). Brown continues to teach the power circuitry receiving enable signals from power control circuitry (collective switched mode power supplies 1-6) to enable the power to deliver the next power level signal via power control circuitry (1-6) (see figs. 1 and 2; column 4, lines 38-52 and column 6, lines 1-11). Brown has the additional feature of disabling power supplies when faults are detected (column 3, lines 41-52).

It would have been obvious to one of ordinary skill of the art having the teachings of Amin and Brown at the time the invention was made, to modify power circuit of Amin to include receiving enable signals from a control circuitry and outputting power signals to processing circuitry as taught by Brown. One of ordinary skill in the art would be motivated to make this combination of having a power circuit receive enable signals from a control circuitry and outputting power signals to processing circuitry in view of the teachings of Brown, as doing so would give the added benefit of disabling power supplies when faults are detected (as taught by Brown above).

Claims 2-5, 7-12 and 15-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Amin and Brown as applied to claims 1, 6 and 14 above, and further in view of Orr et al. (U.S. Patent No. 6,850,048 B2) (hereinafter referred to as Orr).

As to claim 2, Amin in combination with Brown taught a data storage system according to claim 1, as described above. However, neither Amin nor Brown teach the data storage system wherein the packaged microcontroller further includes: a set of built-in analog-to-digital converters coupled to the set of input lines and to the control circuitry, the control circuitry being configured to compare a set of binary values from the set of built-in analog-to-digital converters to a set of pre-determined thresholds to determine when all of the power signals within the set of power signals have reached levels that prevents damage to the storage processing circuitry when the second set of power signals is provided to the storage processing circuitry.

Orr teaches power supply microcontroller (10) that includes: a set of built-in analog-to-digital converters (48) coupled to the set of input lines and to the control circuitry (column 8, lines 55-65), the control circuitry (21 and 22 within 10) being configured to compare a set of binary values from the set of built-in analog-to-digital converters to a set of pre-determined thresholds to determine when all of the power signals within the set of power signals have reached levels that prevents damage to the storage processing circuitry when the second set of power signals is provided to the storage processing circuitry (Orr teaches input state machines 43 within the control circuits 21 and 22 receiving measured values that are received from A/D converters 48 and compared to a threshold; column 10, line 54 thru column 11, line 7). Orr has the additional feature of having the ability to control a relatively arbitrary number of power supplies from various manufacturers with arbitrary voltage levels and varying sequences (column 2, lines 30-36).

It would have been obvious to one of ordinary skill of the art having the teachings of Amin, Brown and Orr at the time the invention was made, to modify microcontroller of Orr to

include analog-to-digital converters and having the control circuitry of the microcontroller compares measured values to thresholds as taught by Orr. One of ordinary skill in the art would be motivated to make this combination of including analog-to-digital converters within the microcontroller and having the control circuitry of the microcontroller compares measured values to thresholds in view of the teachings of Orr, as doing so would give the added benefit of having the ability to control a relatively arbitrary number of power supplies from various manufacturers with arbitrary voltage levels and varying sequences (as taught by Orr above).

As to claim 3, Amin in combination with Brown and Orr taught a data storage system according to claim 2, as described above. Orr further teaches the data storage system wherein the packaged microcontroller further includes: memory (36) which stores pre-loaded code having a version identifier, the control circuitry being configured to: compare the version identifier of the pre-loaded code with a version identifier of available new code, and replace the pre-loaded code stored in the memory with the available new code when the version identifier of the available new code indicates that the available new code is newer than the pre-loaded code, and maintain the pre-loaded code within the memory when the version identifier of the available new code indicates that the available new code is not newer than the pre-loaded code (column 8, lines 32-35 and column 10, line 43 thru column 11, line 7 and column 12, lines 4-15).

As to claim 4, Amin in combination with Brown and Orr taught a data storage system according to claim 3, as described above. Orr further teaches the data storage system includes: a dedicated memory location, wherein the control circuitry, when replacing the pre-loaded code stored in the memory with the available new code, is configured to: set the dedicated memory location with a flag to indicate that a code replacement routine is in progress, overwrite the pre-

loaded code stored in the memory with the available new code, and clear the dedicated memory location to remove the flag to indicate that no code replacement routine is in progress (column 8, lines 32-35 and column 12 line 48 thru column 13, line 11).

As to claim 5, Amin in combination with Brown and Orr taught a data storage system according to claim 2, as described above. Brown further teaches the data storage system further comprising: a power button (inherently comprises a power button); wherein the packaged microcontroller further includes a persistent memory, the control circuitry being configured to: access the persistent memory to determine whether the power button of has been toggled to an "ON" position or an "OFF" position (RESTART or turned off), and place the storage processing circuitry in one of (i) a normal operating state when the persistent memory indicates that the power button has been toggled to the "ON" position, and (ii) a recovery state when the persistent memory indicates that the power button has been toggled to the "OFF" position (column 10,line 60 thru column 11, line 13).

As to claim 7, Amin in combination with Brown taught a packaged microcontroller according to claim 6, as described above. However, neither Amin nor Brown teach the packaged microcontroller further comprising: a set of built-in analog-to-digital converters coupled to the set of input lines and to the control circuitry, the control circuitry being configured to compare a set of binary values from the set of built-in analog-to-digital converters to a set of pre-determined thresholds to determine when all of the power signals within the set of power signals have reached levels that prevents damage to the storage processing circuitry when the second set of power signals is provided to the storage processing circuitry.

Orr teaches power supply microcontroller (10) that includes: a set of built-in analog-to-digital converters (48) coupled to the set of input lines and to the control circuitry (column 8, lines 55-65), the control circuitry (21 and 22 within 10) being configured to compare a set of binary values from the set of built-in analog-to-digital converters to a set of pre-determined thresholds to determine when all of the power signals within the set of power signals have reached levels that prevents damage to the storage processing circuitry when the second set of power signals is provided to the storage processing circuitry (Orr teaches input state machines 43 within the control circuits 21 and 22 receiving measured values that are received from A/D converters 48 and compared to a threshold; column 10, line 54 thru column 11, line 7). Orr has the additional feature of having the ability to control a relatively arbitrary number of power supplies from various manufacturers with arbitrary voltage levels and varying sequences (column 2, lines 30-36).

It would have been obvious to one of ordinary skill of the art having the teachings of Amin, Brown and Orr at the time the invention was made, to modify microcontroller of Orr to include analog-to-digital converters and having the control circuitry of the microcontroller compares measured values to thresholds as taught by Orr. One of ordinary skill in the art would be motivated to make this combination of including analog-to-digital converters within the microcontroller and having the control circuitry of the microcontroller compares measured values to thresholds in view of the teachings of Orr, as doing so would give the added benefit of having the ability to control a relatively arbitrary number of power supplies from various manufacturers with arbitrary voltage levels and varying sequences (as taught by Orr above).

As to claim 8, Amin in combination with Brown and Orr taught a packaged microcontroller according to claim 7, as described above. Orr further teaches the packaged microcontroller comprising: memory (36) which stores pre-loaded code having a version identifier, the control circuitry being configured to: compare the version identifier of the pre-loaded code with a version identifier of available new code; and replace the pre-loaded code stored in the memory with the available new code when the version identifier of the available new code indicates that the available new code is newer than the pre-loaded code, and maintain the pre-loaded code within the memory when the version identifier of the available new code indicates that the available new code is not newer than the pre-loaded code (column 8, lines 32-35 and column 10, line 43 thru column 11, line 7 and column 12, lines 4-15).

As to claim 9, Amin in combination with Brown and Orr taught a packaged microcontroller according to claim 8, as described above. Orr further teaches the packaged microcontroller further comprising: a dedicated memory location, wherein the control circuitry, when replacing the pre-loaded code stored in the memory with the available new code, is configured to: set the dedicated memory location with a flag to indicate that a code replacement routine is in progress, overwrite the pre-loaded code stored in the memory with the available new code, and clear the dedicated memory location to remove the flag to indicate that no code replacement routine is in progress (column 8, lines 32-35 and column 12 line 48 thru column 13, line 11).

As to claim 10, Amin in combination with Brown and Orr taught a packaged microcontroller according to claim 7, as described above. Orr further teaches the packaged microcontroller further comprising: a dedicated memory (36) location; and memory having a

main portion which stores pre-loaded main code and a secondary portion which stores pre-loaded secondary code, wherein the control circuitry is further configured to: access the dedicated memory location to determine whether a flag is set to indicated that a code replacement routine is in progress, and run (i) the pre-loaded main code stored in the main portion of the memory when the dedicated memory location is not set with the flag, and (ii) the secondary code stored in the secondary portion of the memory when the dedicated memory location is set with the flag (column 8, lines 32-35 and column 10, line 43 thru column 11, line 7 and column 12, lines 4-15).

As to claim 11, Amin in combination with Brown and Orr taught a packaged microcontroller according to claim 7, as described above. Brown further teaches the packaged microcontroller wherein the data storage system has a power button, and wherein the packaged microcontroller further comprises: a persistent memory the control circuitry being configured to: access the persistent memory to determine whether the power button of has been toggled to an "ON" position or an "OFF" position (RESTART or turned off), and place the storage processing circuitry in one of (i) a normal operating state when the persistent memory indicates that the power button has been toggled to the "ON" position, and (ii) a recovery state when the persistent memory indicates that the power button has been toggled to the "OFF" position (column 10,line 60 thru column 11, line 13).

As to claim 12, Amin in combination with Brown and Orr taught a packaged microcontroller according to claim 11, as described above. Brown further teaches the packaged microcontroller wherein the control circuitry is further configured to: prior to placing the storage processing circuit in one of the normal operating state and the recovery state, communicate with another packaged microcontroller to determine whether other storage processing circuitry of the

data storage system is entering a normal operating state or a recovery state (column 10, line 60 thru column 11, line 13).

As to claim 15, Amin in combination with Brown taught a method according to claim 14, as described above. However, neither Amin nor Brown teach the method further includes a set of built-in analog-to-digital converters coupled to the set of input lines, and wherein receiving the first set of power signals includes: comparing a set of binary values from the set of built-in analog-to-digital converters to a set of pre-determined thresholds to determine when all of the power signals within the set of power signals have reached levels that prevents damage to the storage processing circuitry when the second set of power signals is provided to the storage processing circuitry.

Orr teaches power supply microcontroller (10) that includes: a set of built-in analog-to-digital converters (48) coupled to the set of input lines and to the control circuitry (column 8, lines 55-65), the control circuitry (21 and 22 within 10) being configured to compare a set of binary values from the set of built-in analog-to-digital converters to a set of pre-determined thresholds to determine when all of the power signals within the set of power signals have reached levels that prevents damage to the storage processing circuitry when the second set of power signals is provided to the storage processing circuitry (Orr teaches input state machines 43 within the control circuits 21 and 22 receiving measured values that are received from A/D converters 48 and compared to a threshold; column 10, line 54 thru column 11, line 7). Orr has the additional feature of having the ability to control a relatively arbitrary number of power supplies from various manufacturers with arbitrary voltage levels and varying sequences (column 2, lines 30-36).

It would have been obvious to one of ordinary skill of the art having the teachings of Amin, Brown and Orr at the time the invention was made, to modify microcontroller of Orr to include analog-to-digital converters and having the control circuitry of the microcontroller compares measured values to thresholds as taught by Orr. One of ordinary skill in the art would be motivated to make this combination of including analog-to-digital converters within the microcontroller and having the control circuitry of the microcontroller compares measured values to thresholds in view of the teachings of Orr, as doing so would give the added benefit of having the ability to control a relatively arbitrary number of power supplies from various manufacturers with arbitrary voltage levels and varying sequences (as taught by Orr above).

As to claim 16, Amin in combination with Brown taught a method according to claim 15, as described above. Orr further teaches the method wherein the packaged microcontroller includes memory (36) which stores pre-loaded code having a version identifier, and wherein the method further comprises: comparing the version identifier of the pre-loaded code with a version identifier of available new code; and replacing the pre-loaded code stored in the memory with the available new code when the version identifier of the available new code indicates that the available new code is newer than the pre-loaded code, and maintaining the pre-loaded code within the memory when the version identifier of the available new code indicates that the available new code is not newer than the pre-loaded code (column 8, lines 32-35 and column 10, line 43 thru column 11, line 7 and column 12, lines 4-15).

As to claim 17, Amin in combination with Brown taught a method according to claim 16, as described above. Orr further teaches the method wherein replacing the pre-loaded code stored in the memory with the available new code includes: setting a dedicated memory location with a

flag to indicate that a code replacement routine is in progress; overwriting the pre-loaded code stored in the memory with the available new code; and clearing the dedicated memory location to remove the flag to indicate that no code replacement routine is in progress (column 8, lines 32-35 and column 12 line 48 thru column 13, line 11).

As to claim 18, Amin in combination with Brown taught a method according to claim 15, as described above. Orr further teaches the method wherein the microcontroller includes memory (36) having a main portion which stores pre-loaded main code and a secondary portion which stores pre-loaded secondary code, and wherein the method further comprises: accessing a dedicated memory location to determine whether a flag is set to indicated that a code replacement routine is in progress; and running (i) the pre-loaded main code stored in the main portion of the memory when the dedicated memory location is not set with the flag, and (ii) the secondary code stored in the secondary portion of the memory when the dedicated memory location is set with the flag (column 8, lines 32-35 and column 10, line 43 thru column 11, line 7 and column 12, lines 4-15).

As to claim 19, Amin in combination with Brown taught a method according to claim 15, as described above. Brown further teaches the method wherein the data storage system has a power button (inherently comprises a power button), and wherein the method further comprises: accessing a persistent memory to determine whether the power button of has been toggled to an "ON" position or an "OFF" position (RESTART or turned off); and placing the storage processing circuitry in one of (i) a normal operating state when the persistent memory indicates that the power button has been toggled to the "ON" position, and (ii) a recovery state when the

persistent memory indicates that the power button has been toggled to the "OFF" position (column 10,line 60 thru column 11, line 13).

As to claim 20, Amin in combination with Brown taught a method according to claim 19, as described above. Brown further teaches the method further comprises: prior to placing the storage processing circuit in one of the normal operating state and the recovery state, communicating with another packaged microcontroller to determine whether other storage processing circuitry of the data storage system is entering a normal operating state or a recovery state (column 10, line 60 thru column 11, line 13).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Sugent whose telephone number is (571) 272-5726. The examiner can normally be reached on 8AM - 4PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at (866) 217-9197 (toll-free). If you would

like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or (571) 272-1000.

James Sugent
Patent Examiner, Art Unit 2116
July 20, 2006

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100